



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER OF PATENTS AND TRADEMARKS  
Washington, D.C. 20231  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/784,965	02/16/2001	Joseph Fjelstad	TESSERA 3.0-085 CONT DIV	5441

530 7590 06/20/2002

LERNER, DAVID, LITTENBERG,  
KRUMHOLZ & MENTLIK  
600 SOUTH AVENUE WEST  
WESTFIELD, NJ 07090

EXAMINER

CHAMBLISS, ALONZO

ART UNIT	PAPER NUMBER
----------	--------------

2827

DATE MAILED: 06/20/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/784,965

Applicant(s)

FJELSTAD, JOSEPH

Examiner

Alonzo Chambliss

Art Unit

2827

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 2/28/02(amendment A).
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-3 and 5-20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-3 and 5-20 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☒ The proposed drawing correction filed on 15 February 2002 is: a) ☒ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other:

### **DETAILED ACTION**

1. Amendment A filed on 2/15/02 has been fully considered and made of record as Paper No. 10.

#### ***Response to Arguments***

2. Applicant's arguments with respect to claims 1-3 and 5-20 have been considered but are moot in view of the new ground(s) of rejection.

Kitano discloses a continuous mass of dielectric material 6, since the dielectric material has an uninterrupted space when the material partially encapsulates the first microelectronic element and fully encapsulates the second microelectronic element.

#### ***Drawings***

3. The corrected or substitute drawings were received on 2/15/02 as Paper No. 8. These drawings are approved by the examiner.

#### ***Claim Rejections - 35 USC § 102***

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-4, and 7 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Yamaguchi (U.S. 5,157,475).

With respect to Claim 1, Yamaguchi teaches a microelectronic element 51 (i.e. semiconductor chip) having a front face including contacts (i.e. located at the end of bonding wire 53) with a back surface remote there from and edges extending there between. The mass of dielectric material 55 at least partially encapsulates the microelectronic element 51. The conductive units 54 embedded in the mass of dielectric material 55 along at least one microelectronic element edge. At least some of the conductive units 54 are exposed on oppositely facing exterior surfaces of the mass of dielectric material 55, wherein at least some of the conductive units 54 include a pad portion (i.e. connecting portion) 54a exposed at the bottom surface of the dielectric material 55 and a protrusion 54b extending from the pad portion 54a. The protrusion 54b is exposed at the top surface of the dielectric material 55, wherein each of the protrusion 54b extends from a portion of the associated pad portion furthest from the microelectronic element 51. The conductive elements 54 extend through the dielectric material 55 and electrically interconnect the contacts with the conductive units (see col. 11-63; Fig. 5b). Giving the teaching of the above product, claim 1 is clearly anticipated by Yamaguchi.

With respect to claim 2, Yamaguchi teaches a dielectric material 55 having a top exterior surface juxtaposed with the front face of the microelectronic element 51 and a bottom exterior surface juxtaposed with the back surface of the microelectronic element 51. Some of the conductive units 54 are exposed at both the top and bottom exterior

surfaces of the dielectric material 55 (see Fig. 5b). Giving the teaching of the above product, claim 2 is clearly anticipated by Yamaguchi.

With respect to Claim 3, Yamaguchi teaches that the cross sectional area of each of the protrusion 61 is smaller than the cross sectional area of the pad portion (i.e. the portion that is bonded to wire 53) associated with the protrusion 61 (see Fig. 9c). Giving the teaching of the above product, claim 3 is clearly anticipated by Yamaguchi.

With respect to Claim 4, Yamaguchi teaches protrusions 54 extend from a portion of the associated pad portion 54a furthest from the microelectronic element 51 (see Fig. 5b). Giving the teaching of the above product, claim 4 is clearly anticipated by Yamaguchi.

With respect to Claim 7, Yamaguchi teaches the conductive units 54 protrude from the top exterior surface (see Fig. 5b). Giving the teaching of the above product, claim 7 is clearly anticipated by Yamaguchi.

### ***Claim Rejections - 35 USC § 103***

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 5, 6, 9-12, 14, 18, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaguchi (U.S. 5,157,475) and Melton et al. (U.S. 5,844,315) as applied to claims 1, 2 and 8 above, and further in view of Kitano et al. (U.S. 5,608,265).

With respect to Claim 5, Yamaguchi discloses attaching the first assembly to another external device (see col. 4 lines 47-58). Furthermore, to form a second microelectronic assembly instead of just one would readily be recognized to one skilled in the art, since in the absent of new and unexpected results the duplication of parts is obvious. The court held that mere duplication of parts has no patentable significance unless a new and unexpected result is produced. *In re Harza*, 274 F.2d 669, 124 USPQ 378 (CCPA 1960). Therefore, it would have been obvious to one skilled in the art that a second assembly when incorporated with Yamaguchi would allow the second assembly being attach to the exposed conductive units at bottom exterior surface of the first assembly are electrically connected to the exposed conductive units at the top exterior surface of the second assembly as taught by Yamaguchi.

Yamaguchi fails to disclose a substrate underlying the bottom exterior surface of the second assembly, wherein the exposed conductive units of the second assembly are connected to the substrate. However, with respect to Claim 6, Melton discloses a substrate 40 underlying the bottom exterior surface of first assembly 10, wherein the exposed conductive units 46 of the first assembly are connected to the substrate 40 (see Figs. 6 and 7). Since, one skilled in the art in light of Yamaguchi knows that the first and second assemblies can be attached to one another and that any one of the assemblies can be called a first or second assembly. Therefore, it would have been obvious to one skilled in the art to incorporate the substrate 40 with Yamaguchi, since the substrate would create a low-profile microelectronic assembly as taught by Melton.

With respect to Claim 8, Melton discloses the back surface of the microelectronic element 12 is exposed at an exterior surface of the assembly (see Fig. 6).

With respect to Claim 9, Yamaguchi discloses thermally conductive adhesive (i.e. Ag paste) attached to back surface of the microelectronic device (see col. 4 lines 11-13).

Yamaguchi-Melton both fail to disclose conductive units having hollow centers, wherein the hollow centers extend through the conductive units. A reflowable conductive material exposed at one of the exterior surfaces of the assembly. However, With respect to Claims 10 and 11, Kitano discloses some of the conductive units 4-1, 4-2, 4-3 having hollow centers 7, wherein the hollow centers extend through the conductive units 4-1, 4-2, 4-3 (see Figs. 2-5). Therefore, it would have been obvious to incorporate the hollow conductive units with Yamaguchi, since the hollow conductive units would improve the electrical connection between plural assemblies as taught by Kitano.

With respect to Claims 12 and 13, Kitano discloses a reflowable conductive material 5 is exposed at one of the exterior surfaces of the assembly (see Figs. 2-5).

With respect to Claims 14 and 18, Kitano discloses a first microelectronic element 1 in 14-d has a front face including contacts and a back surface remote therefrom. A second microelectronic element 1 in 14-c is juxtaposed with the front face of the first microelectronic element 1 and having terminals thereon. The mass of dielectric material 6 is at least partially encapsulating the first microelectronic element 1 and fully encapsulating the second microelectronic element 1. The conductive units 5 secured to

the mass of dielectric material 6. The conductive elements 3 extend through the dielectric material 6 and electrically interconnect the contacts and the terminals with the conductive units 5 with each other, wherein one or more of the conductive units 5 are exposed at an exterior surface of the assembly (see Figs. 2-5 and 10).

8. Claims 14-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Kitano et al. (U.S. 5,608,265).

With respect to Claims 14 and 18, a first microelectronic element 1 in 14-d has a front face including contacts and a back surface remote there from. A second microelectronic element 1 in 14-c is juxtaposed with the front face of the first microelectronic element 1 and having terminals thereon. The mass of dielectric material 6 is at least partially encapsulates the first microelectronic element 1 and fully encapsulates the second microelectronic element 1. The conductive units 5 secured to the mass of dielectric material 6. The conductive elements 3 extend through the dielectric material 6 and electrically interconnect the contacts and the terminals with the conductive units 5 with each other, wherein one or more of the conductive units 5 are exposed at an exterior surface of the assembly (see Figs. 2-5 and 10).

With respect to Claims 15-17, the second microelectronic element 1 includes a face surface having terminals and a back surface remote there from, wherein the back surface faces and is attached to the front surface of the first microelectronic element 1 by the conductive units 5 (see Fig. 10).

With respect to Claim 19, a thermally conductive adhesive 15 is attached to the back surface of the first microelectronic element 1 by the chip pad 2 (see Fig. 11).



The prior art made of record and not relied upon is cited primarily to show the product of the instant invention.

***Conclusion***

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning the communication or earlier communications from the examiner should be directed to Alonzo Chambliss whose telephone number is (703) 306-9143. The fax phone number for this Group is (703) 308-7722 or 7724.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-7956.

Application/Control Number: 09/784,965  
Art Unit: 2827

Page 9

AC

AC/June 14, 2002



DAVID L. TALBOTT  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2800